

FS-i5005_OP10

Product Specification

Ultra-Low Power 2.4GHZ Wi-Fi +BT5.0 Module

(OPL1000)

Version Ver1.2

History

Document Release	Date	Modification	Initials	Approved
Version V1.0	2021/01/04			
Version V1.1	2021/3/15			
Version V1.2	2021/4/13			

Overview

The OPL1000 SoC features a fully integrated 2.4GHz radio transceiver and baseband processor for Wi-Fi 802.11b and Bluetooth[®] Smart applications. The SoC can be used as a standalone application-specific communication processor or as a wireless data link in hosted MCU systems where ultra-low power is critical. The OPL1000 supports flexible memory architecture for storing profiles, stacks and custom application codes, and can be updated using Over-The-Air (OTA) technology. Qualified Bluetooth Smart protocol stack and Wi-Fi TCP/IP stack are stored in a dedicated ROM. The OPL1000 is equipped with dual processors, ARM[®] Cortex[®]-M0 and M3, for handling different processes. All software runs on the ARM[®] Cortex[®]-M0 processor while more intensive application-specific activities run on the ARM[®] Cortex[®]-M3 processor. The OPL1000 can be connected to any external MCU through SPI, I2C or UART interfaces and sensors or other devices through GPIOs. The transceiver interfaces directly to the antenna and is fully compliant with the Wi-Fi 802.11b and Bluetooth 5.0 BLE standards. With integrated antenna switch, RF balun, power amplifier (PA) and low noise amplifier (LNA), the OPL1000 allows both Wi-Fi and Bluetooth Smart to minimize PCB design area and external component requirement.

Features

The OPL1000 complies with ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

Processors

- ARM[®] Cortex[®]-M3 Application Processor
- ARM[®] Cortex[®]-M0 Link Controller

Wi-Fi

- 802.11b up to 11Mbps
- Supports STA mode
- WPA/WPA2 security supported
- Automatic beacon scanning and discovery
- Built-in TCP/IP stack
- Integrated dual power amplifiers: low (-2 dBm), high (+10 dBm) +

Optional internal T/R switch by-pass mode available to increase to +12dBm

Bluetooth Smart

- Compliant with Bluetooth 5.0 BLE specifications with 2Mbps rate capability
- Slave mode support
- Adaptive Frequency Hopping (AFH)
- All GATT-based profiles supported
- Built-in BLE stack
- Max. 8 concurrent BLE connections supported
- 2 to 12 dBm transmit output power
- -80 dBm receive sensitivity

Memories

- 4kb One-Time-Programmable (OTP) memory
- 384 kB System SRAM
- 768 kB ROM

HW Crypto Engine

- AES-128/256 bits Encryption
- P-192/256 ECDH (Elliptic Curve Diffie-Hellman) Key Generation
- SHA2
- TRNG

Power Management

- Integrated Buck DC-DC converter
- Supports coin cell and alkaline battery

Clock

- Built-in low power 32KHz RC oscillator and support optional 32KHz crystal.
- Optional external 32 kHz crystal (± 150 ppm max) and built-in low power oscillator

General purpose, capture and sleep timers

FW OTA (Over-The-Air) update support

Digital Interfaces

- General purpose I/Os: 24
- Two UARTs with hardware flow control up to 3Mbps
- Three SPI+™ interfaces
- One I2C bus at 100 kHz, 400 kHz

Analog Interfaces

- 10-bit Auxiliary ADC inputs up to 16 channels
- Six GPIO pins with 16mA driving capability
- Six PWMs

Radio Transceiver

- Fully integrated dual-mode 2.4 GHz CMOS transceiver
- Single wire antenna: no external matching and no external T/R switch required

Current Consumption

- Real Time Clock (RTC) mode with always-on domain alive < 5uA
- Deep sleep current ~ 3 uA1
- Timed sleep current ~4 uA2
- Supply current at battery terminal (with DC-DC) †
 - o Wi-Fi 802.11b:
 - Tx ~ 18mA @ -2 dBm; 115mA @ +10 dBm
 - Rx ~ 17.5 mA
 - o Bluetooth Smart:
 - Tx ~ 12 mA @ 2 dBm; 63 mA @ +12 dBm
 - Rx ~ 12 mA

Optional internal T/R switch by-pass mode available to increase to +12dBm

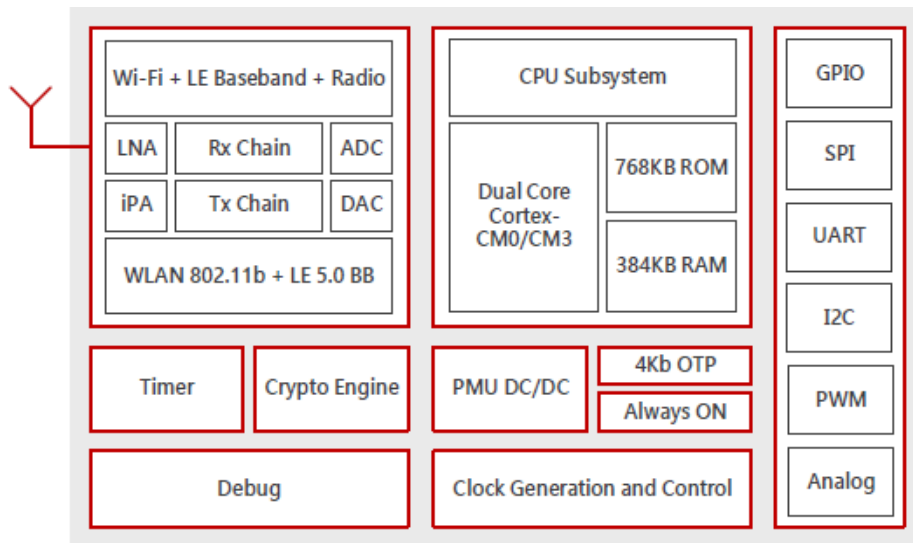
Package

- 48-pin QFN, 6 mm x 6 mm

Flash

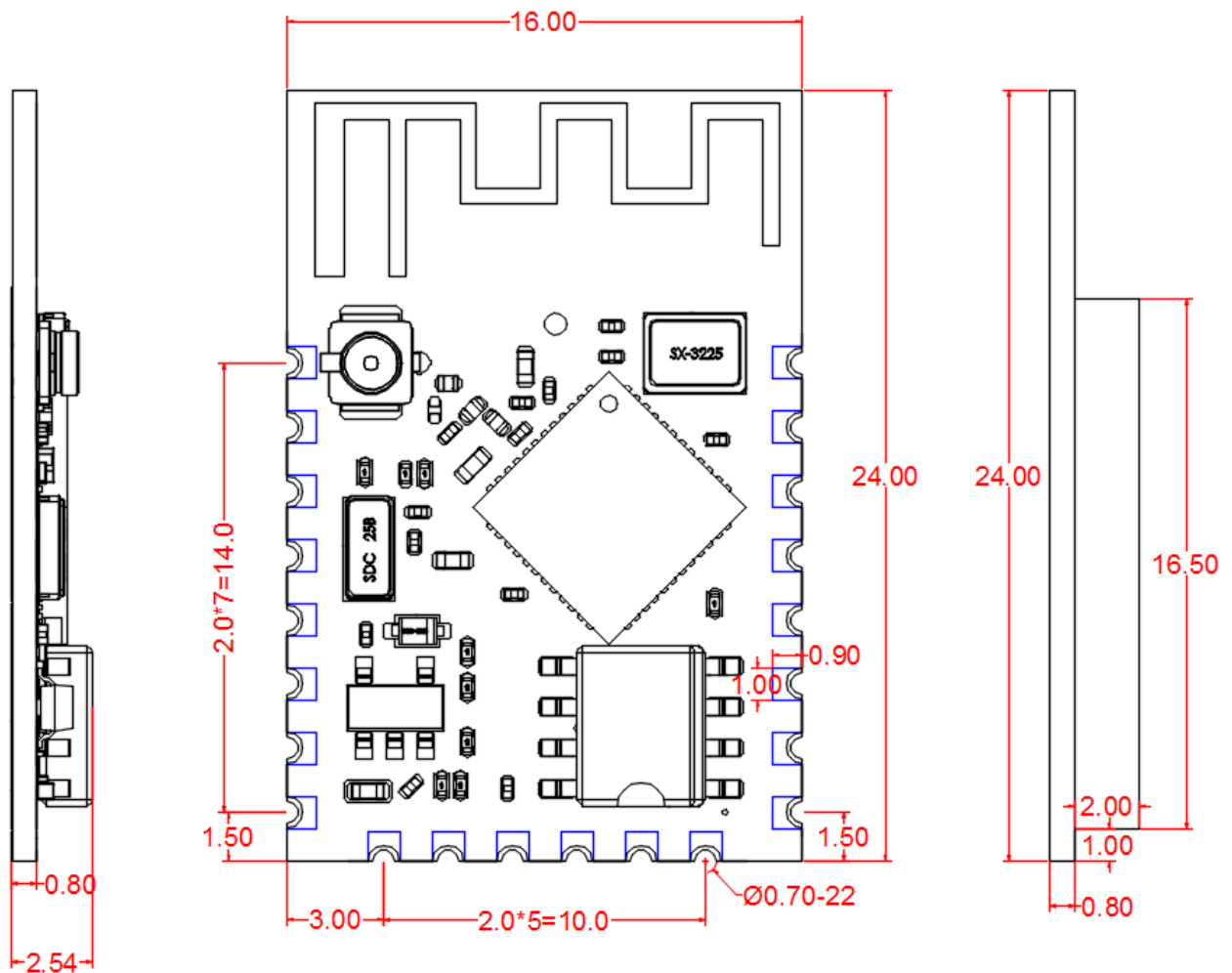
- Module internal expansion 8Mbit SPI Flash

Block Diagram



Module Size

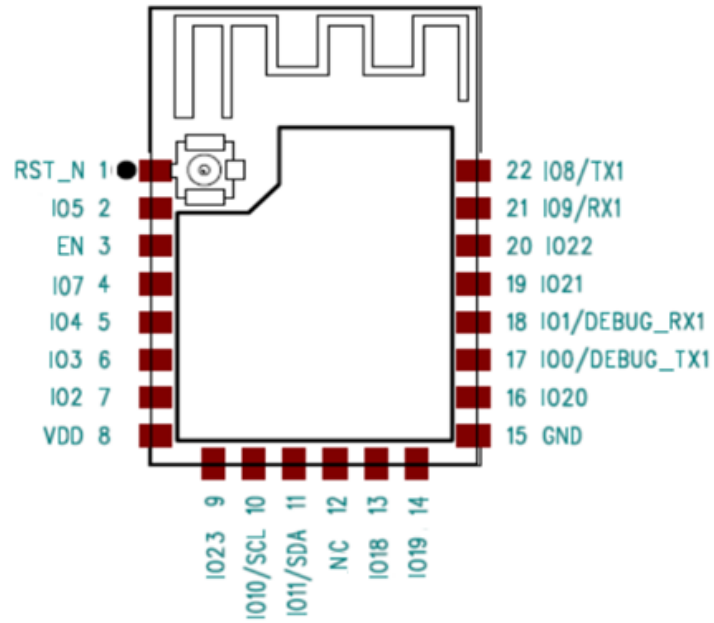
Unit: mm



Side view without shield

Front view

Side view with shield



Pin Description

PIN	FUNCTION	Description
PIN1	RST_N	Reset
PIN2	IO5	GPIO_5
PIN3	EN	Enable reset pin (active high), connected to RST_N inside the module
PIN4	IO7	GPIO_7
PIN5	IO4	GPIO_4
PIN6	IO3	GPIO_3
PIN7	IO2	GPIO_2
PIN8	VDD	Power
PIN9	IO23	GPIO_23
PIN10	IO10/SCL	GPIO_10
PIN11	IO11/SDA	GPIO_11
PIN12	NC	NC
PIN13	IO18	GPIO_18
PIN14	IO19	GPIO_19
PIN15	GND	GND
PIN16	IO20	GPIO_20
PIN17	IO0/TX	GPIO_0/Communication transmission serial port, default programming,
PIN18	IO1/RX	GPIO_1/ Communication receiving serial port, default programming, Debug port
PIN19	IO21	GPIO_21
PIN20	IO22	GPIO_22
PIN21	IO9/RX	GPIO_9/ Communication receiving serial port, default AT port
PIN22	IO8/TX	GPIO_8/ Communication transmitting serial port, default AT port

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Battery Supply	VDD_BAT			3.8	V
RF LDO Supply	DCDC_IN			1.59	V
PA Supply	VDD_PA			3.8	V
OTP Programming Supply	VDDQ			2.75	V
Digital Core Supply	VDD			1.35	V
IO Supply	VDDO			3.8	V
Operating Ambient Temperature	TO	-30		70	°C
Storage Temperature	TS	-40		125	°C
Junction temperature	TJ			125	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Battery Supply ⁺¹	VDD_BAT	2.0		3.6	V
RF LDO Supply	DCDC_IN	1.2	1.32	1.5	V
PA Supply ⁺¹	VDD_PA	2.0		3.6	V
OTP Programming Supply ⁺²	VDDQ	2.25	2.5	2.75	V
Digital Core Supply	VDD	1.08	1.2	1.32	V
IO Supply	VDDO	2.0		3.6	V

1 Application voltage under 2.7v will degrade RF performance

2 VDDQ should be kept low or floating except during programming. Maximum accumulative time for the entire macro exposed under 2.5 +/- 10% should be less than 1 second.

Wi-Fi RF specification

Parameter	Mode & Condition	Min	Typ	Max	Unit
Frequency Range		2400		2500	MHz
Input Impedance			50		Ω
Input Reflection				-10	dB
Rx Max Input Level	DSSS 2Mb/s. FER<8%. MPDU = 1024 octets	-6			dBm
	HR/DSSS 11Mb/s. FER<8%. MPDU = 1024 octets	-9.5			dBm
Rx Sensitivity	DSSS 1Mb/s, FER<8%, MPDU = 1024 octets			-91	dBm
	HR/DSSS 11Mb/s. FER<8%. MPDU = 1024 octets			-80	dBm
Adjacent Channel Rejection	≥30MHz separation, Pwanted = Psens+6dB, DSSS 2Mb/s, FER<8%, MPDU = 1024 octets	35			dB
	≥25MHz separation, Pwanted = Psens+6dB, HR/DSSS 11Mb/s, FER<8%, MPDU = 1024 octets	35			dB
Tx Output Power	@ Low Power (LP)		0	-2	dBm
	@ High Power (HP)		8	10	dBm
Tx EVM	DQPSK, peak			-21	dB

Bluetooth RF specification

LE Receiver

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity	BLE, 1Mbps, 0.1% BER			-80 [†]	dBm
Max Input Power	BLE, 1Mbps, 0.1% BER			-20	dBm
C/I Co-Channel	$P_{\text{wanted}} = -67\text{dBm}$, BLE, 0.1% BER		6		dB
C/I $\pm 1\text{MHz}$ Adjacent Channel	$P_{\text{wanted}} = -67\text{dBm}$, BLE, 0.1% BER		-4		dB
C/I $\pm 2\text{MHz}$ Adjacent Channel	$P_{\text{wanted}} = -67\text{dBm}$, BLE, 0.1% BER		-31		dB
C/I $\geq 3\text{MHz}$ Adjacent Channel	$P_{\text{wanted}} = -67\text{dBm}$, BLE, 0.1% BER		-40		dB
Out-Of-Band Blocking	30 MHz ~ 2000 MHz, $P_{\text{wanted}} = -67\text{dBm}$, $f_{\text{wanted}} = 2426\text{MHz}$, 0.1% BER	-5			dBm
	2000 MHz ~ 2400 MHz, $P_{\text{wanted}} = -67\text{dBm}$, $f_{\text{wanted}} = 2426\text{MHz}$, 0.1% BER	-15			dBm
	2500 MHz ~ 3000 MHz, $P_{\text{wanted}} = -67\text{dBm}$, $f_{\text{wanted}} = 2426\text{MHz}$, 0.1% BER	-35			dBm
	3000 MHz ~ 12.5 GHz, $P_{\text{wanted}} = -67\text{dBm}$, $f_{\text{wanted}} = 2426\text{MHz}$, 0.1% BER	-30			dBm
Intermodulation	$P_{\text{wanted}} = -64\text{dBm}$, 0.1% BER, $n=3,4,5$	-34	-29		dBm

LE Transmitter

Parameter	Condition	Min	Typ	Max	Unit
Tx Output Power	Low Power		2	5	dBm
	Gain control range		20		dB
	High Power		12	14	dBm
	Gain Step		2		dB
Tx In-Band Spurious Emissions	@ 0dBm, foffset=2MHz		-53		dBm
	@ 0dBm, foffset=3MHz		-57		dBm
	@ 10dBm, foffset=2MHz		-41		dBm
	@ 10dBm, foffset=3MHz		-45		dBm
Tx Out-Of-Band Spurious Emissions	Narrowband spurious, 30MHz-1GHz			36	dBm
	Narrowband spurious, GHz-12.75GHz			30	dBm

	Narrowband spurious, 1.8GHz-1.9GHz, 5.15GHz-5.3GHz	-47	dBm
	Wideband spurious, 30MHz-1GHz	-86	dBm
	Wideband spurious, 1GHz-12.75GHz	-80	dBm
	Wideband spurious, 1.8GHz-1.9GHz, 5.15GHz-5.3GHz	-97	dBm
LO Performance	Initial carrier frequency tolerance ,	-150	150 KHz
Frequency Drift	Frequency drift	50	50 KHz
	Drift rate		20 kHz/50 μ s
Frequency Deviation	Average deviation in payload (sequence used is 00001111)	225	275 KHz
	Maximum deviation in payload (sequence used is 10101010)	185	KHz
	Channel spacing	2	MHz

Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times

